## Claims

[c1] 1. A stack-type multi-chip package structure, comprising:

a substrate;

a first chip with a first active surface having a plurality of first bonding pads and a plurality of first bump pads thereon and a first backside, wherein the first bonding pads are positioned in the peripheral region on the first active surface and the first bump pads are positioned on the first active surface, and the backside of the first chip is attached to the substrate:

a plurality of first conductive wires, wherein one end of each first conductive wire is electrically connected to one of the first bonding pads and the other end of the first conductive wire is electrically connected to the substrate; a second chip with a second active surface having a plurality of second bonding pads thereon and a second backside, wherein the second bonding pads are positioned in the peripheral region on the second active surface, and the second chip assembles with the first active surface of the first chip such that the second backside faces the first chip;

a plurality of second bump pads set up on the second

backside of the second chip, wherein the second bump pads are fabricated using a metallic material; a plurality of bumps positioned between the first chip and the second chip such that one end of the bumps are bonded to the first bump pads and the other end of the bumps are bonded to the second bump pads; a plurality of second conductive wires, wherein one end of the second conductive wire is electrically connected to one of the second bonding pads and the other end of the second conductive wire is electrically connected to the substrate; and a packaging material encapsulating the first chip, the second chip, the bumps, the first conductive wires and the second conductive wires.

- [c2] 2. The package structure of claim 1, wherein material constituting the second bump pads comprises gold.
- [c3] 3. The package structure of claim 1, wherein material constituting the bumps comprises gold.
- [c4] 4. The package structure of claim 1, wherein material constituting the bumps comprises lead-tin alloy.
- [c5] 5. The package structure of claim 1, wherein material constituting the bumps comprises lead-free alloy.
- [c6] 6. The package structure of claim 5, wherein material

constituting the bumps comprises tin-silver-copper alloy.

- [c7] 7. The package structure of claim 1, wherein the bumps are positioned in the peripheral region of the first active surface close to the first bonding pads.
- [08] 8. The package structure of claim 1, wherein the second chip is larger than the first chip in size.
- [c9] 9. A chip structure having bumps thereon, comprising: a chip with an active surface having a plurality of bonding pads thereon and a backside; at least a bump pad set up on the backside of the chip, wherein the bump pad is fabricated using a metallic material; and at least a bump attached to the bump pad.
- [c10] 10. The chip structure of claim 9, wherein material constituting the bump comprises lead-tin alloy.
- [011] 11. The chip structure of claim 9, wherein material constituting the bump comprises lead-free alloy.
- [c12] 12. The chip structure of claim 11, wherein material constituting the bump comprises tin-silver-copper alloy.
- [c13] 13. The chip structure of claim 9, wherein material constituting the bump pad comprises gold.

- [c14] 14. The chip structure of claim 9, wherein material constituting the bump comprises gold.
- [c15] 15. A method of fabricating bumps on the backside of a chip, comprising the steps of: providing a chip with an active surface having a plurality of bonding pads thereon and a backside; forming at least a bump pad on the backside of the chip; and attaching a bump to the bump pad.
- [c16] 16. The method of claim 15, wherein the step of forming the bump pad on the backside of the chip further comprises:

  forming a metallic layer on the backside of the chip; and patterning the metallic layer to form the bump pad.
- [c17] 17. The method of claim 15, wherein the step of forming the bump pad on the backside of the chip further comprises:

  putting a mask on the backside of the chip, wherein the

putting a mask on the backside of the chip, wherein the mask has at least an opening so that the backside of the chip is exposed;

forming a metallic layer over the mask and the exposed backside of the chip; and

removing the mask so that the remaining metallic layer

on the backside of the chip becomes the bump pad.

- [c18] 18. The method of claim 15, wherein before forming the bump pad on the backside of the chip, the method further comprises forming a protective film on the active surface of the chip.
- [c19] 19. The method of claim 15, wherein the chip further comprises a passivation layer coated on the backside of the chip so that the passivation layer is removed before forming the bump pad on the backside of the chip.
- [c20] 20. The method of claim 15, wherein during the step of attaching bumps to the bump pads, patterning and electroplating process, a printing process, a bump-bonding process by a wire-bonding machine or a ball-implanting process are performed.